COMMON SPACER DUAL GATE MEMORY CELL AND METHOD FOR FORMING A NONVOLATILE MEMORY ARRAY

ABSTRACT OF THE DISCLOSURE

In a common spacer dual gate memory cell formed on a semiconductor substrate, two gates for two transistors with a spacer therebetween are arranged in series between two bit lines, and two isolated word lines for the respective gates preferably extends in the directions perpendicular to each other, in which one of the two gates includes a silicon nitride for gate dielectric, and the other gate dielectric also includes a silicon nitride or an oxide only. With the novel structure, up to four charge storage locations are achieved between each pair of the bit lines.